

Multifunctional Devices and Logic Gates With Undoped Silicon Nanowires

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We report on the electronic transport properties of multiple-gate devices fabricated from undoped silicon nanowires. Understanding and control of the relevant transport mechanisms was achieved by means of local electrostatic gating and temperature dependent measurements. The roles of the source/drain contacts and of the silicon channel could be independently evaluated and tuned. Wrap gates surrounding the silicide-silicon contact interfaces were proved to be effective in inducing a full suppression of the contact Schottky barriers, thereby enabling carrier injection down to liquid-helium temperature. By independently tuning the effective Schottky barrier heights, a variety of reconfigurable device functionalities could be obtained. In particular, the same nanowire device could be configured to work as a Schottky barrier transistor, a Schottky diode or a p-n diode with tunable polarities. This versatility was eventually exploited to realize a NAND logic gate with gain well above one.

Nanometer-scale electronic devices fabricated from silicon nanowires (SiNWs) are drawing significant attention in view of their potential application in electronics¹, optoelectronics² and biochemical sensing^{3,4}. The transport properties and the functionality of such electronic devices are usually controlled by doping. In most cases, the incorporation of doping impurities in SiNWs is obtained *in-situ* during nanowire growth⁵, but a precise control over their spatial distribution^{6,7} and their activation⁸ has not been achieved yet. Doping control becomes a particularly critical issue when the characteristic device size approaches the nanometer scale, *i.e.* comparable to the typical distance between dopants for standard doping levels (10^{17} - 10^{19} cm⁻³). In this limit, device performances can depend on only a few dopants^{9,10}, and be extremely sensitive to their precise locations, leading to a significant device-to-device variability. The main obstacle coming from the use of undoped nanowires lies in the difficulty to form low-resistance contacts due to the unavoidable presence of a Schottky barrier (SB)¹¹ at the metal-silicon interface. Therefore, understanding and controlling the properties of electrical contacts to SiNWs is of fundamental importance¹². Here, we investigate the properties of metal-silicide contacts to undoped SiNWs, and we study the possibility to obtain largely-tunable contact resistances through a combination of two fabrication processes: a controlled silicidation of the metal-SiNW contacts and the fabrication of local gate electrodes wrapped around each silicon-silicide interface. We demonstrate that contact resistances can be largely suppressed with gate voltages of the order of 1 V, enabling measurable carrier injection down to 4K. In addition, through local electrostatic doping of the SiNW,

our approach provides the possibility to implement different functionalities within the same SiNW device, which can work as a bipolar transistor, a Schottky diode or p-n diode with gate-tunable polarities. Finally, we provide as well an example of how two such devices could be programmed to operate as a NAND logic gate.

We used undoped SiNWs grown by chemical vapor deposition via a catalytic vapor-liquid-solid method (growth details were given in an earlier work¹³). Our sample fabrication process relies on a few steps of e-beam lithography, e-beam metal deposition, and lift-off. Initially, alignment markers and ordered arrays of 500-nm-wide Cr/Al (10/5 nm) gate electrodes, spaced by 500 nm, are defined on top of an oxidized heavily doped silicon substrate (p^{++} Si/SiO₂). Successively, after a brief sonication in isopropanol, the as-grown undoped SiNWs are released from their growth substrate and drop-casted on the device substrate. Wires crossing a couple of bottom gates are identified by means of scanning electron microscopy (SEM) and contacted with 120-nm-thick nickel electrodes to be used as source and drain contacts. The bottom gates are also contacted in the same lithographic step. Prior to the Ni deposition, the native oxide on the SiNWs is etched away by dipping the sample for 5s in buffered HF. This step removes also the Al cap layer of the bottom gates leaving the underlying Cr layer unaffected. After contacting the SiNWs a double step thermal annealing process is performed in order to promote the silicidation of the contacts. Temperature and annealing times are calibrated in order to obtain the protrusion of the nickel silicide along the nanowire¹⁴ from the Ni contacts to the bottom gates. The preparation of the sample is completed with the deposition of 80-nm-thick Al top gates overlapping with the bottom gates and, simultaneously, an additional top gate electrode crossing the middle region of the SiNW. The Al top gates are electrically isolated from the nanowire by a preliminary deposition and oxidation of four 1.5-nm-thick Al layers. Each layer is fully oxidized by leaving the sample in the load-lock chamber of the e-beam evaporator under an oxygen pres-

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sure of 200 Torr for 10 minutes. Due to their large overlapping area and to the small thickness of the (native) oxide interlayer, each bottom gate and the corresponding top gate are effectively shorted together, resulting in a wrap-gate geometry¹⁵.

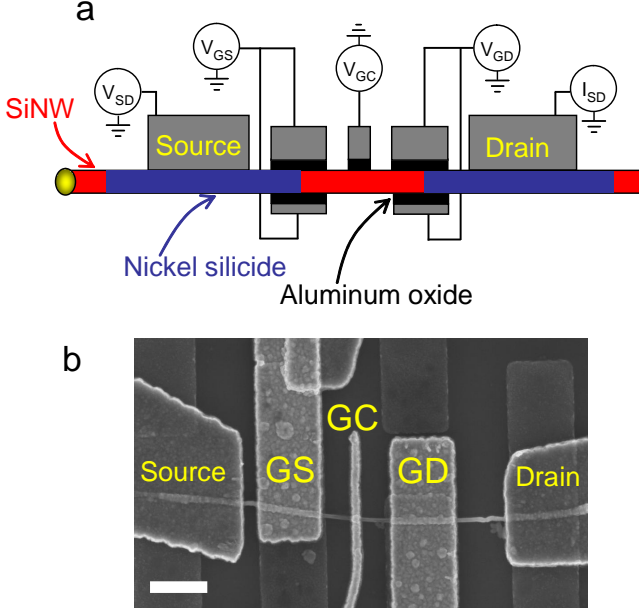


FIG. 1. a) Schematic of a multi-gate device made from a single, undoped SiNW. Two wrap-gates, labeled as GS and GD, are designed to control the Schottky barriers at the silicide-silicon junctions formed by the source and drain contacts. The finger gate in the middle, labeled as GC, is meant to control carrier population in the silicon channel. b) SEM micrograph of the device. Scale bar: 400nm.

The SiNW device and its schematics are shown in 1. Since the nickel silicide sections have a metallic character, SB contacts are formed at the silicon-silicide interfaces. The wrap-gate electrodes, labelled as GS and GD, are designed to embed these interfaces and to control the respective SBs. We shall refer to these electrodes as to the *contact gates*. The wrap-gate geometry maximizes the gating efficiency. The finger-shape gate, labelled as GC, is meant to control carrier population in the channel. We shall refer to this electrode as to the *channel gate*.

The multiple gate layout enables independent control of the different device sections, *i.e.* the SB contacts and the channel. We shall begin by evaluating their relative contributions under different gating conditions and, for each case, we shall investigate the relevant transport mechanisms. At room temperature and for zero gate voltages, thermionic emission over the contact SBs is the dominant transport process. Since the Fermi level of the nickel silicide is pinned below the silicon mid-gap, *i.e.* closer to the valence band, transport across each silicide-silicon junction is dominated by the thermionic emission of holes over the p-type SB. The application of

negative voltages to the contact-gates GS/GD produces a local band bending that reduces the thickness of the SB of the corresponding silicide-silicon junction. This enables the onset of thermally assisted tunneling through the barrier top-edge leading to a reduction of the effective p-type SB height^{16,17}, ϕ . We find that negative contact-gate voltages of a few V are sufficient to induce a strong suppression of ϕ . This is apparent from 2(a) where the source-drain current, I_{SD} , is plotted as a function of the source-drain bias voltage, V_{SD} , for two gating conditions. The green characteristic corresponds to $V_{GS} = -3.2$ V and $V_{GD} = 0$. In this case, the effective SB at the source contact is suppressed and the device behaves as a Schottky diode whose polarity is imposed by the SB at the drain contact. The blue characteristic corresponds to the reversed gating condition, *i.e.* $V_{GD} = -3.2$ V and $V_{GS} = 0$, which results in an opposite diode polarity. In both cases the channel gate was set to -2.5 V in order to get rid of any possible barrier in the channel (see discussion further below). Appreciable quantitative discrepancies can be noted in the two characteristics of 2(a). Under reverse-bias polarization, described by the qualitative band diagrams in the two insets of 2(a), the measured current is dominated by the thermally assisted tunneling of holes across the reverse-bias SB, *i.e.*

$$I_{SD} = A^* S T^2 \exp\left(-\frac{e\phi}{k_B T}\right) \quad (1)$$

where $k_B = 8.617\text{eV/K}$ is the Boltzmann constant, A^* is the Richardson constant, T is the temperature, e is the absolute value of the electronic charge, S is the cross-sectional area of the conducting silicon channel. From a ratio of ~ 50 between the reverse currents of the green and the blue characteristics, we estimate that the drain SB height exceeds the source SB height by $k_B T \ln(50) \approx 0.1\text{eV}$.

In order to independently measure the two effective SB heights and to study their gate-voltage dependence, the sample was loaded in a home-made variable-temperature insert. For each gate-voltage setting, temperature was varied between 220 K and 370 K in steps of 10 K. The effective barrier height was extracted from the temperature dependence of the reverse-bias current using the thermionic-emission relation (1) (ϕ is given by the slope of the Arrhenius plot $\ln(I_{SD}/T^2)$ vs $1/T$). The results are shown in 2(b), where the effective SB heights are plotted as a function of the corresponding contact-gate voltages. The two data sets reveal approximately linear gate-voltage dependences with same slopes. This denotes almost identical capacitive couplings to the respective contact gates. The drain SB height is 0.35 eV for $V_{GD} = 0$ and it vanishes for $V_{GD} = -2.8\text{V}$. The source SB height for $V_{GD} = 0$ could not be directly measured due to the limited upper temperature of our setup. Yet a linear extrapolation of the data in 2(b) yields a source SB height of 0.45 eV for $V_{GD} \rightarrow 0$. This confirms the 0.1 eV difference with the drain SB height previously deduced from the ratio of the reverse currents in 2(a). Because

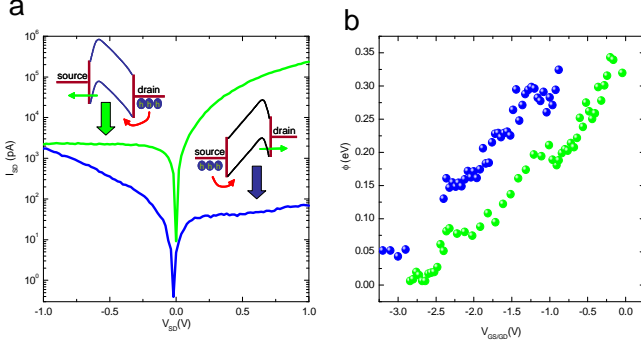


FIG. 2. Schottky-diode $I_{SD}(V_{SD})$ characteristics obtained for two gate settings. The blue trace is obtained with $V_{GD} = -3.2$ V and $V_{GS} = 0$. In this configuration, the drain effective SB is suppressed while the source SB is left unaltered, thereby leading to rectifying behaviour. The green trace is obtained with $V_{GS} = -3.2$ V and $V_{GD} = 0$, resulting in an opposite rectifying behavior. Insets: schematic band diagrams illustrating the thermal emission of carriers over the reverse-bias Schottky contact. b) Contact-gate dependence of the effective (p-type) SB height for the source (blue symbols) and the drain (green symbols) contacts. The horizontal axis refers to V_{GS} and V_{GD} , respectively.

of this difference, the source SB requires slightly more negative gate voltages to be entirely suppressed.

If both the effective SBs are simultaneously suppressed by sufficiently negative voltages applied to the respective contact gates, transport across the device becomes entirely dependent on the hole population of the silicon channel¹⁸. We find that current transport is dominated by the thermionic emission of holes over a potential barrier formed by the downward bending of the valence band edge. The emission of carriers over this barrier is purely thermionic as opposed to the case of the contact SBs where the onset of tunnelling leads to a smaller effective barrier. Following a similar procedure as before, we have measured the height of this barrier as a function of V_{GC} . The results are shown by solid dots in 3, where each dot is the result of a fit to an Arrhenius plot.

All data points were taken at constant $V_{SD} = -1$ V. A room-temperature $I_{SD}(V_{GC})$ characteristic, taken in the same V_{GC} range, is also shown on a logarithmic scale (red trace). The two data sets meet fairly well the proportionality relation expected from the thermionic-emission relation (1). The measured barrier height is ~ 0.11 eV for $V_{GC} = 0$ V and it decreases linearly for negative gate voltages. Below $V_{GC} < -1.5$ V, the barrier becomes too small to be reliably extracted from the Arrhenius plot (in this regime, transport is no longer thermally activated). A saturation of the $I_{SD}(V_{GC})$ characteristic is consistently observed below this threshold voltage.

The complete suppression of the silicon-channel barrier, together with the suppression of the effective SBs

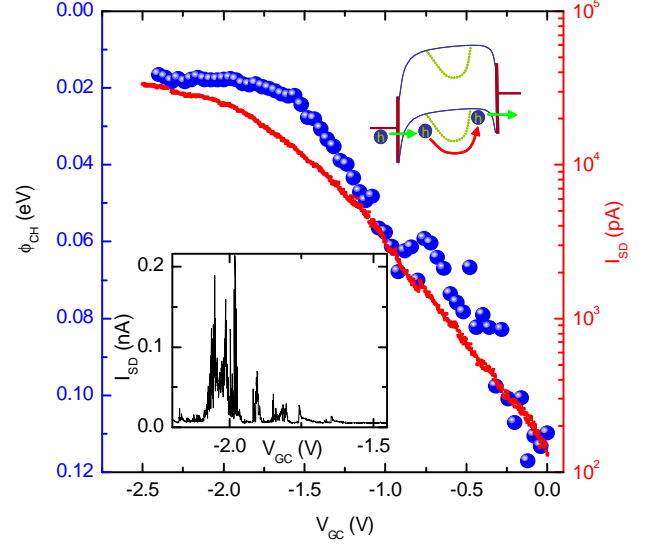


FIG. 3. The effective SBs of the source and drain contacts are simultaneously suppressed by setting $V_{GS} = V_{GD} = -3.2$ V. As a result, the device can be operated as a p-type field-effect transistor, using the channel-gate voltage, V_{GC} , to modulate the source-drain current, I_{SD} . Red trace: transfer characteristic, $I_{SD}(V_{GC})$, taken with $V_{SD} = 100$ mV at room temperature. Blue symbols: channel barrier height, ϕ_{CH} , as a function of V_{GC} . Upper inset: schematic band diagram illustrating the thermal emission of holes over the gate-controlled barrier in the middle region of the silicon channel (green dotted line). Lower inset: $I_{SD}(V_{GC})$ characteristic taken for $V_{SD} = 100$ mV at $T = 4$ K.

at the silicon-silicide contacts, are further confirmed by low temperature measurements. An $I_{SD}(V_{GC})$ characteristic taken at $T = 4$ K for $V_{SD} = 0.1$ V is shown in the lower inset of 3. While I_{SD} is unmeasurably small for $V_{GC} > -1.6$ V, pronounced current oscillations can be seen below this threshold, providing evidence of low-temperature transport through an undoped silicon device. The observed current oscillations are due to the Coulomb blockade effect. Their irregular structure reflects single-hole tunneling through a series of hole islands formed along the nanowire as it is typically observed in disordered low-dimensional conductors.

So far we have shown full control of hole transport in an undoped SiNW device. The same device could be operated as a p-type field-effect transistor, a Schottky diode, or a multi-island single-hole tunneling device. We pointed out that the p-type character of all these functionalities arises from the pinning of the silicide Fermi energy closer to the silicon valence band edge. At the same time, our thermionic-emission measurements revealed that the SB height can exhibit appreciable contact-to-contact variations within the same

device. These variations can arise from the atomic structure of the silicide-silicon junction^{19–23} as well as from the field effect of trapped charges in the periphery of the silicide-silicon junction^{12,24}.

Given the relatively large variability (~ 0.1 eV) in the SB height of silicon-silicide contacts, it is possible to have SiNW devices where Fermi level pinning occurs close to the silicon mid-gap, yielding p-type and n-type SBs relatively close to each other and to the half-gap value (0.55 eV). These types of devices exhibit bipolar behavior and, as a result, they can give rise to a larger range of functionalities. 4(a) shows the bipolar field-effect characteristic of one of such devices with a gate layout identical to that of 1, except for the absence in this case of the channel-gate electrode. The horizontal axis refers to both contact-gate voltages being swept together.

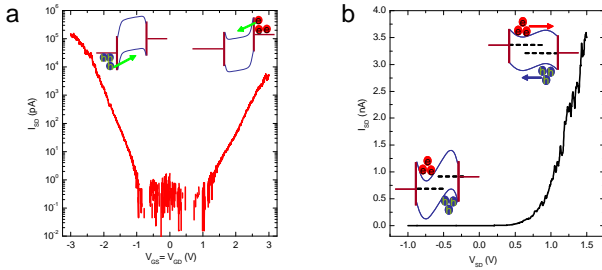


FIG. 4. a) Room-temperature transfer characteristic of a dual-gate device showing bipolar transistor behavior. Hole-dominated (electron-dominated) transport is observed for negative (positive) gate voltages, as schematically shown in the left (right) inset. This measurement was taken with $V_{SD} = 0.5$ V and $V_{GS} = V_{GD}$. b) $I_{SD}(V_{SD})$ characteristic showing the rectifying behavior expected for an electrically doped p-n diode. The tunable “doping” is achieved with $V_{GS} = 2$ V and $V_{GD} = -2$ V. Schematic band diagrams for forward and reverse-bias conditions are shown in the upper and lower insets, respectively.

A more interesting behaviour is observed when the two gates are polarized at opposite voltages, fixed with respect to the corresponding (source or drain) contacts. 4(b) shows that, in this case, the device behaves like an electrostatically doped p-n diode. As opposed to the case of true p-n diodes, here the built-in potential arises from static charges accumulated on the contact-gate electrodes^{25–28} and not on the potential of the ionized impurities in the space-charge region. In the forward bias polarization the side of the nanowire populated with holes has a higher electrochemical potential than the side populated by electrons. The barriers created by the contact gate become smaller and can be surmounted by thermally activated carriers as shown in the upper inset of 4(b). This results in a diffusion current of holes from the p-like to the n-like region and an electron current in the opposite direction. In the case of reverse bias polarization, transport of electrons and holes is hindered by the

high potential barriers created by the contact gates as depicted in the lower inset of 4(b).

Below we show that dual-gate SiNW devices, having Schottky contacts well coupled to the respective gates, can serve as building blocks for logic circuits. Bottom-up logic gates based on carbon nanotubes^{29,30} or semiconductor nanowires^{3,31} have already been reported, along with more complex circuits like ring oscillators³² extending digital operation into the high frequency domain. Here we demonstrate the implementation of a NAND device made from two dual-gate SiNW devices connected in series as in 5(a). Since the SiNWs are undoped, this approach has the advantage of not requiring complementary doping. A NAND device performs an AND and a NOT operation in series. It accepts two input voltages corresponding to the binary values 0 and 1 and it delivers a single output voltage according to the truth table in 5(b). In our circuit, the voltage level $V = 0$ V corresponds to a logical 0, while the voltage level $V = -1$ V corresponds to a logical 1.

Let us now analyze the operating principle of this NAND device, by considering the different input configurations. When the two input gates controlling $GS2$ and $GD2$ are at logical 0, the input stage is in a highly resistive state due to both SBs being simultaneously high. As a consequence the bias voltage, $V_{cc} = -1.2$ V, falls mostly across the feedback stage and the output terminal acquires a value $V_{out} \approx V_{cc}$ corresponding to a logical 1. The presence of an electrical connection between the output terminal and the contact gate $GD1$ produces a positive feedback, since a negative value on the contact gate suppresses the corresponding effective SB, making the impedance of the feedback stage lower and hence forcing V_{out} even closer to V_{cc} , i.e. to logical output 1. When, on the contrary, both inputs are at logical 1, the input stage attains a low-resistive state due to the simultaneous suppression of both effective SBs. As a result, the output voltage approaches a logical 0, and V_{cc} falls mainly on the feedback stage. Because of the feedback line, $V_{out} \approx 0$ V enforces a high value of the SB at the drain contact of the feedback stage. This increases its resistance with respect to the input stage, thereby reinforcing logical output 0. In the intermediate regimes, when one of the two inputs is at logical 0 and the other is at logical 1, one gated SB is suppressed while the other is not. In this case, the presence of the feedback line is crucial in producing a stable configuration with $V_{out} \approx V_{cc}$, i.e. logical output 1. In fact, under this condition both of the effective SBs at the source and drain contacts of the feedback stage are suppressed leading to a lower impedance as compared to the input stage. As a result, the output voltage is stabilized at a logical 1.

Since in actual logic circuits the output of a logic gate can serve as the input of another gate, an important figure of merit for logic gates is gain, g , defined as the slope of the linear portion of the output characteristic. A high-gain logic gate ($g > 1$) has the capability to drive another logic gate without the need of signal restoration. From

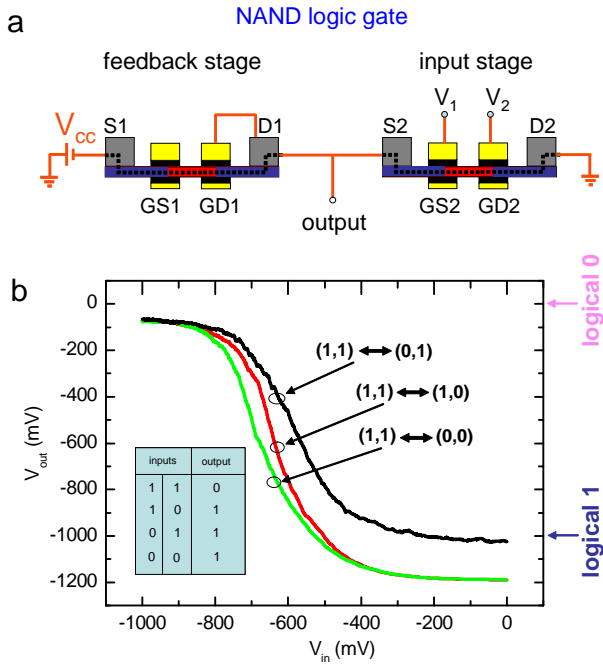


FIG. 5. a) Schematic of a NAND logic gate based on two dual-gate SiNW devices. One device acts as an input stage, while the second one acts as a feedback stage to enforce the correct output voltage. The two input lines are fed to the contact gates GS2 and GD2. The output line is taken from the D1 contact, which is shorted with the S2 contact. The feedback function is accomplished by applying a fixed negative polarization of -3 V to GS1, large enough to suppress the corresponding effective SB, and by connecting GD1 to the output terminal. A voltage $V_{cc} = -1.2$ V is applied to S1, with D2 at ground. b) Output characteristics of the logic gate. The black trace, obtained with $V_{in} = V_1$ and $V_2 = -1$ V, corresponds to the transition $(1,1) \leftrightarrow (0,1)$ in the input levels. The red trace, obtained with $V_{in} = V_2$ and $V_1 = -1$ V, corresponds to the transition $(1,1) \leftrightarrow (1,0)$. The green trace, obtained with $V_{in} = V_1 = V_2$, corresponds to the transition $(1,1) \leftrightarrow (0,0)$. Inset: truth table for a NAND logic gate.

the data in 5(b) we find g between 2.6 and 4.7. In addition, the NAND gate requires relatively low voltage levels as compared to previously reported logic gates built from semiconductor nanowires^{3,31}. Similar to other earlier works²⁹, our NAND device was assembled from two dual-gate devices connected via external leads. Yet we should like to point out that the same logic gate could be obtained with a single nanowire using a common electrode for D1 and S2.

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